

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-586003	Application No. 10/802,991
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Lawrence D. Wong	
		Filing Date March 16, 2004	Group Art Unit 1792

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA						
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Foreign Patent Documents or Published Foreign Patent Applications								
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							Yes	No
	AD							
	AE							
	AF							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AG	Baklanov, M.R., et al., "Comparative study of Porous SOG Films with Different Non-Destructive Instrumentation", <i>Proceedings of the IEEE 2001 International Interconnect Technology Conference</i> , pp. 189-191, June 2001.
	AH	Drage, J.S., et al., "Effects of Electron Beam Exposure on Poly(arylene Ether) Dielectric Films", <i>Mat. Res. Soc. Symp. Proc.: Low-Dielectric Constant Materials III</i> , vol. 476, pp. 121-128, April 1997.
	AI	Feiler, D., et al., "E-Beam Curing Process of Low- κ Dielectrics for Unlanded Vias in 0.25 μ m CMOS Technology", <i>Proc. 5th International Dielectrics for ULSI Multilevel Interconnection Conference (DUMIC)</i> , Catalog No. 99IMIC-44D, pp. 289-294, February 1999.
	AJ	Kawamura, S., et al., "New Measurement Technique of Pore Size Distribution of Porous Low- κ Film", <i>Proceedings of the IEEE 2001 International Interconnect Technology Conference</i> , pp. 195-197, June 2001.
	AK	Lee, H.-J., et al., "Characterization of Porous Low- κ Dielectric Thin Films Using X-Ray Reflectivity, Small Angle Neutron Scattering and Ion Scattering", <i>Proceedings of the IEEE 2001 International Interconnect Technology Conference</i> , pp. 247-249, June 2001.
	AL	Lee, H.-J., et al., "A Novel and Low Thermal Budget Planarization Scheme for Pre-Metal Dielectric Using Electron-Beam Cured HSQ (Hydrogen Silsesquioxane) in STC (Stacked Capacitor) DRAM", <i>Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials</i> , pp. 502-503, September 1999.
	AM	Licata, T.J., et al., "Interconnect Fabrication Processes and the Development of Low-Cost Wiring for CMOS Products", <i>IBM Journal of Research and Development</i> , 39(4):419-435, July 1995.
	AN	Matsuki, N., et al., "Aurora Low- κ PECVD Deposited SiOC Films for Copper Dual Damascene Interconnect Applications", ASM International, ASME Presentation November 2001, 24 pages.

Examiner Signature	Date Considered
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